IN THE CLAIMS

1. (withdrawn) A ROM embedded DRAM, comprising:

a DRAM array having a first portion of ROM cells and a second portion of DRAM cells;

wherein the ROM cells are formed by programming DRAM cells within the DRAM array; and

correction circuitry fabricated on and integrated with the DRAM.

2. (withdrawn) The ROM embedded DRAM of claim 1, wherein the correction circuitry is hard coded.

3. (withdrawn) The ROM embedded DRAM of claim 1, wherein the correction circuitry is error correcting code circuitry.

4. (withdrawn) The ROM embedded DRAM of claim 1, wherein the error correction circuitry is parity checking circuitry.

5. (withdrawn) The ROM embedded DRAM of claim 1, wherein the error correction circuitry is chosen from a group consisting of:

parity, Hamming code, modified Hamming code, Gray code, polynomial checking, and cyclical redundancy checking.

6. (withdrawn) A method of fabricating a ROM embedded DRAM, comprising:

forming an array of DRAM cells having a first portion of ROM cells and a second portion of DRAM cells;

programming a ROM portion of the DRAM cells as ROM bits; and

encoding the ROM bits in error correction circuitry.

7. (withdrawn) The method of claim 6, wherein encoding comprises:

encoding with ECC circuitry.

8. (withdrawn) The method of claim 6, wherein encoding comprises:

encoding with parity checking circuitry.

9. (currently amended) A method of operating a ROM embedded DRAM, comprising:
receiving a row and column address to read data from a ROM section;
reading an encoded ROM bit;
correcting the read ROM bit if necessary with on-chip error correcting circuitry; and
presenting the corrected ROM bit as output data.

10. (currently amended) The method of claim 9, wherein correcting comprises:
decoding the read ROM bit with the on-chip error correcting circuitry;
comparing the decoded ROM bit with the actual ROM bit; and
correcting if the decoded ROM bit differs from the read ROM bit.

11. (previously presented) The method of claim 10, wherein decoding comprises:
error correcting with ECC circuitry.

12. (original) The method of claim 11, wherein error correcting with ECC circuitry comprises:
generating an ECC corrected ROM bit from a read ROM bit;
comparing the ECC corrected bit with the read ROM bit; and
correcting the read ROM bit if the ECC corrected ROM bit and the read ROM bit do not match.

13. (original) The method of claim 10, wherein decoding comprises:
error correcting with parity checking.

14. (original) The method of claim 13, wherein error correcting with parity checking comprises:
comparing the parity check bit with the read ROM bit; and
inverting the read ROM bit if the parity bit indicates an error.

15. (withdrawn) A ROM embedded DRAM, comprising:

a DRAM array having a first portion of ROM bits and a second portion of DRAM bits; and

an error correction element containing encoded ROM bit data for each ROM bit.

16. (withdrawn) The ROM embedded DRAM of claim 15, wherein the error correction element is error correcting code (ECC) circuitry.

17. (withdrawn) The ROM embedded DRAM of claim 15, wherein the error correction element is parity checking circuitry.

18. (withdrawn) A method of repairing ROM bit errors in a ROM embedded DRAM, comprising:

programming a ROM section of a ROM embedded DRAM;

encoding ROM data in error correction circuitry;

determining whether the ROM bit data is correct; and

correcting the ROM bit data if the ROM bit data and the stored data are different.

19. (withdrawn) The method of claim 18, wherein determining whether the ROM bit data is correct comprises:

decoding the ROM data; and

comparing the decoded ROM data to the read ROM data.

20. (withdrawn) The method of claim 19, wherein decoding the ROM data is performed by error correction circuitry (ECC).

21. (withdrawn) The method of claim 19, wherein decoding the ROM data is performed by parity checking circuitry.

22. (withdrawn) A method of correcting ROM bit errors in a ROM embedded DRAM, comprising:

programming a ROM section of a ROM embedded DRAM;

encoding on the ROM embedded DRAM in error correcting code (ECC) circuitry the ROM data;

decoding read ROM data before presenting the data to a user; and

correcting the ROM data if the ROM bit data if the ROM bit data is in error.

23. (withdrawn) The method of claim 22, wherein the error correcting code circuitry is chosen from a group consisting of:

parity, Hamming code, modified Hamming code, Gray code, polynomial checking, and cyclical redundancy checking.

24. (currently amended) A method of operating a ROM embedded DRAM, comprising:

receiving a row and column address to read data from a ROM section;

reading a byte of ROM data using an on-chip error correcting code decoder;

correcting the read ROM bit if necessary; and

presenting the corrected ROM bit as output data.

25. (original) The method of claim 24, wherein reading a byte of ROM data using error correcting code comprises:

reading a byte of ROM data;

decoding the byte of ROM data; and

determining if the ROM data is correct.

26. (currently amended) The method of claim 25, wherein decoding is performed by on-chip decoding circuitry chosen from a groups consisting of:

parity, Hamming code, modified Hamming code, Gray code, polynomial checking, and cyclical redundancy checking.